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EXAMINER	
GOSSAGE, GLENN A	
ART UNIT	**PAPER NUMBER**
2187	19

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/752,594	Applicant(s) KENDALL ET AL.	
	Examiner Glenn Gossage	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to telephone communication(s) ~~filed~~ on *23 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. A Request for Continued Examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 10, 2004 has been entered.

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on October 6, 2003 have been approved by the Examiner, subject to drafting review. Corrected drawings are REQUIRED in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance. While proposed drawing corrections showing changes in red were submitted, it does not appear replacement sheets of drawings were ever submitted.

3. It is once again noted that the disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

In the (amended) paragraphs beginning on page 37, line 13, at line 4 of the insertion, it appears "or procedures" should be changed to --for procedure-- for clarity. Similarly, on page 39, lines 12 and 17, it appears --for procedure-- should be inserted before "320" for clarity and consistency, since the use of different names (process flow, procedure, technique, etc) for the

same reference numeral 320 is confusing. See also page 41, line 4, as well as the last paragraph on page 41 (as amended in the response filed October 6, 2003). Additionally, on page 40, line 18, it appears "technique 320" should be changed to --technique or procedure 320-- in order to use a consistent terminology or notation with respect to the reference numeral 320.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected. Note that many of these issues/objections were not addressed, by way of either amendment or argument, in the response filed October 6, 2003.

In the claims:

In claim 5, line 4, it appears "verification" should be changed to --verifying-- for consistency (note the "verification" in claim 1, line 4 and the "verifying" in claim 2, line 1, e.g.). See also claim 6, line 4.

In claim 8, line 2, it appears "the" should be deleted for clarity. Also, --the-- should be reinserted before "memory" (both occurrences) for clarity and consistency (note claims 7 and 9, e.g.).

In claim 17, line 1, "the" (either occurrence) should be deleted for clarity.

Appropriate correction is required.

4. Claims 2-6, 13, 14 and 17-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, and therefore its dependent claims, the language "by a processor 'other than' the memory" is somewhat confusing as it is not readily apparent how a "memory" is a "processor" (in this regard, compare the clearer language of claim 14). Moreover, claim 3 is then somewhat unclear as it is not clear how claim 3 further limits claim 2 (if the processor is "other than" the memory as set forth in claim 2, the processor would appear to be an "external" processor). [In this regard, also see 35 U.S.C. 112, fourth paragraph.] Also, the proper antecedent for "the verification" in claim 3 is not entirely clear (note the "verification" in claim 1, line 4 and the "verifying" in claim 2, line 1, e.g.). [Should "processor other than" in claim 2, line 2 be changed to --verification processor which is not within--, and claim 3 deleted (similar to claim 15)? Note that "processor other than the memory" in claim 5, line 4 and claim 6, lines 4-5 should then be changed to --verification processor-- for clarity and consistency.]

In claim 13, and therefore its dependent claims, the relationship between the "automation circuitry" and the "special programming circuitry" is not adequately clear. [Should "disabled; a" in lines 4-5 be changed to --disabled, said automation circuitry including--, for clarity? See Figures 4 and 5.] Note that this issue was addressed, by way of either amendment or argument in the response filed May 10, 2004. In this regard, attention is respectfully directed to 37 CFR 1.111.

In claim 17, the proper antecedent for "the memory" in lines 5-6 is also not entirely clear since there are two memories set forth in the claims. Similarly, in lines 5-6, the proper

antecedent for "the words" is not entirely clear (note claim 13, line 9 and claim 17, lines 5 and 6, e.g.). It appears "a" in line 6 should be changed to --the--, and "the" in line 6 changed to --those-- for clarity. Note also that it appears "the" (first occurrence) in line 5 should be changed to --a-- for clarity (to avoid possible antecedent problems with "the plurality of words programmed in a second memory," e.g.).

Similarly, in claim 18, line 1, it appears "if any one of the plurality of" should be changed to --programmed into the memory if any one of those words-- or other similar language for clarity (to avoid possible antecedent problems, e.g.) and consistency.

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-14 and 17-24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of copending Application No. 09/748,825. Although the conflicting claims are not identical, they are not patentably distinct from each other because the commonly assigned copending application claims a method and apparatus for programming a memory, the method including entering a

special programming mode of a memory that disables internal program verification by the memory, the memory including automation circuitry for program verification, programming a plurality of words into the memory without the memory performing internal program verification, and exiting the special programming mode of the memory, and the deletion or removal of limitations or steps such as those directed to enabling internal program verification would have been readily obvious to those of ordinary skill in the art at the time the claimed invention was made. That is, since the commonly assigned copending patent application anticipates the claim elements as set forth in the present claims, the present invention is seen to be obvious in light of the claims of the commonly assigned patent application, anticipation being the epitome of obviousness. See particularly claims 1-2, 15-16 and 22-23, for example. Note also that the commonly assigned patent application also claims subsequently enabling internal program verification, as well as having a host processor verify external to the memory the programming of the plurality of data words into the memory. The commonly assigned patent application also claims disabling entry into the special program mode of the memory, as well as using only a single programming pulse for each bit of each word of the plurality of words, and sending a data word to the memory for reprogramming.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 1-14 and 17-24 are also rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No.

6,732,306. Although the conflicting claims are not identical, they are not patentably distinct from each other because the commonly assigned patent claims a method and apparatus for performing programming operations in a memory as in the present invention, the method including entering a special programming mode of a memory that disables internal program verification by the memory, the memory including automation circuitry for program verification, programming a plurality of words into the memory without the memory performing internal program verification, and exiting the special programming mode of the memory. See particularly claims 1, 14 and 17, for example. The commonly assigned patent also claims enabling internal program verification, as well as programming a plurality of words, and using a host processor as a "verification processor" to verify the programming during a special programming mode. Since the commonly assigned patent anticipates the claim elements as set forth in the present claims, the present invention is seen to be obvious in light of the claims of the commonly assigned patent, anticipation being the epitome of obviousness.

Applicants' indication in the response filed May 10, 2004 that "terminal disclaimers will be submitted when the present application is in condition for allowance" (response at page 11) is noted. However, an indication that a terminal disclaimer "will be submitted" is not a proper response to a double patenting rejection based on an issued U.S. patent (as opposed to a provisional double patenting rejection based on a copending application). A proper response to a (non-provisional) double patenting rejection is the filing of a terminal disclaimer; cancellation of the conflicting claims; or the presentation of arguments explaining why the claims are not believed to be obvious. This is necessary in order to clearly and fully develop the issues in the

prosecution record and to avoid possible future prosecution delays. Note also that the application will not be in condition for allowance when there are outstanding rejections.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 and 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Intel Corporation Application Note AP-629 or AP-678, each taken separately, in view of Olivo et al.

With respect to claim 1, as well as claim 13, a method for programming a memory including enabling a "special" or test programming mode of a memory by entering a special programming access code in a state controller, wherein the memory includes automation circuitry for program verification, was known in the art at the time the claimed invention was made. See, for example, Intel Corporation Application Note AP-629 or AP-678, each taken separately. As one of ordinary skill in the art would readily appreciate, a plurality of words may be programmed into the memory during a "special" or test mode, and the "special" or test programming mode exited after the tests are performed, with the programming modes of the flash memory being controlled by a write state machine in a well known manner (see, for example, page 2, line 21 to page 4, line 8 of the present specification, as well as pages 7-9 and 9-11 of Intel Corporation

Application Note AP-678 and AP-629, respectively). The use of a write state machine allows the sequence of steps necessary to perform a programming operation to be easily controlled or automated. The various modes may be entered by entering a certain command or "code" in a command register which is forwarded to the write state machine(see, particularly, Figure 1 of Application Note AP-678).

Application Note AP-629 also teaches that, in order to reduce programming and testing time of a nonvolatile memory, one should consider modifying the method or program flow to perform only necessary operations (see AP-629, at page 9, as well as page 10 and Figure 4). Application Note AP-629 further teaches that program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations and that one can save time by not performing program verify operations (see AP-629, at page 9, column 2, e.g.).

Application Note AP-678 similarly teaches that verification of each location as it is programmed or written should be eliminated from the programming routines of automated flash memories (see AP-678, at page 9, column 1, e.g., as well as page 10 and Figure 3), since program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations (see AP-678, at page 9, column 2, e.g.).

The Application Notes only specifically discuss saving time by not performing program verify operations with the external ATE , and do not teach disabling internal program verification operations during the "special" programming mode so that a plurality of words are programmed in the "special" or test mode without the memory performing internal program verification.

However, Olivo similarly discloses a method of programming a memory such as a flash nonvolatile memory during a "special" or test programming mode of the memory, and teaches disabling program verification operations by an internal state machine during the "special" programming mode so that a plurality of words may be programmed or tested without the memory performing internal program verification (see column 1, lines 26-62; column 2, lines 9-31; and column 4, lines and 7-12 32-36, e.g.). Olivo teaches that overall testing speed may be improved, and that various testing values or parameters may be selected at will so that the memory test can be made fully independent of the control unit and the internal state machine (see column 5, lines 1-10, as well as column 1, lines 40-62, e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to disable program verification operations by an internal state machine during a "special" programming mode, as taught by Olivo et al, in the flash memory apparatus and method of Intel Corporation Application Note AP-629 or AP-678, each taken separately, so that a plurality of words may be programmed without the memory performing internal program verification, because the Intel Corporation Application Note AP-629 or AP-678, each taken separately, teaches that program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations and that one should consider modifying the method or program flow to perform only necessary operations, and Olivo teaches that an improved testing speed and greater flexibility in the testing process may be obtained by disabling or not performing internal program verification operations. The improvement in testing speed and ability to change the testing process independent of the control unit and internal state machine as taught by Olivo et al provide ample motivation and suggestion

to disable internal program verification operations in a memory such as in the Intel Corporation Application Note AP-629 or AP-678, each taken separately, so as to avoid redundant program verify operations while providing an improved test speed and increased flexibility in the testing process.

With respect to claims 2-3 and 14, one of ordinary skill in the art would readily appreciate that the automated test equipment in the Intel Corporation Application Note AP-629 or AP-678, each taken separately, may include processor and that the memory may be tested by resending a plurality of words previously sent into the memory.

With respect to claims 4-6 and 8, as well as claims 17-18 and 20, internal program verification by the memory may be enabled after the memory is tested so that the user can be assured that data is being properly programmed and is reliable. The programming and testing of nonvolatile memories is an iterative process so that if one of the plurality of words does not verify, the programming and verification are repeated (see page 2, lines 15-20 of the present specification, e.g.). If all of the plurality of words verify, the programming mode may be exited.

As per claims 7 and 19, one of ordinary skill in the art would recognize that the "special" programming mode may be permanently disabled after being tested at the factory so that a user is not able to enter the "special" programming mode.

With respect to claims 9 and 21, one of ordinary skill in the art would recognize that the number of iterations in the programming or testing sequence may obviously be varied. The ability to simply change the testing procedure is a key aspect of the teachings of Olivo et al, and the selection of a single iteration or a single programming pulse in order to quickly test the

memory would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made.

With respect to claims 10-12 and 22-24, the Intel Corporation Application Note AP-629 or AP-678, each taken separately, teaches that programming the plurality of words into the memory may continue until a programming ending condition is met (see page 4, line 14 to page 5, line 3 of the present specification, e.g.). As one of ordinary skill in the art would readily appreciate, the programming ending condition may be that a pre-selected time has elapsed (a "timeout" condition has occurred) or an ending address (the last address in the memory has been reached and the entire memory has been tested).

7. Applicants' arguments filed May 10, 2004 have once again been considered but are not persuasive.

The argument that Olivo teaches disabling the write state machine but does teach or suggest disabling internal program verification operations is not persuasive since the write state machine executes the implementation algorithms for sequencing the high voltage circuitry for performing programming, erase and verification operations (see page 4, lines 1-8 and page 4, line 22 to page 5, line 5, e.g.) and by disabling the write state machine, these operations can also be disabled. Note also that the language "(processor other than) the memory" is somewhat confusing as the term "memory" may be considered to be a memory array or may be considered to include some peripheral circuitry [note that the "memory" (array) 20 in Figure 4 of the present invention is coupled to state machine/control circuitry 28, which are within "memory" 24. Similarly, in

Olivo, the state machine 11 and other control circuitry which selectively enables and disables the state machine may be considered "external" to a "memory."

It is also important to note that the Examiner is not suggesting that the circuitry of Olivo be bodily incorporated into that of Intel Corporation Application Note AP-629 or AP-678. The test of obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In the instant case, the Intel Application Notes teach that external and internal verification operations are redundant and that certain verification operations within a nonvolatile memory should be eliminated from the programming routines of automated flash memories (see Intel Application Note AP-678 at page 9, column 1, e.g.). Olivo specifically teaches excluding or disabling the internal state machine and using other test and control circuits to perform testing and verification in a nonvolatile memory (column 4, lines 7-12, e.g.). The Examiner respectfully submits that the combined teachings of the references, and reasonable inferences which may be drawn therefrom by those of ordinary skill in the art, would have suggested that the internal state machine verification operations within the nonvolatile memory of the Intel Application Notes may be eliminated from the programming routines of the automated flash "memory" so that the test and verification operations may be performed in a fully independent manner and so that the verification operations are not bound by internal time constraints, Olivo

teaching that the testing of nonvolatile memories in such a manner is compatible with known nonvolatile memories and permits the use of the same circuitry (column 5, lines 1-10).

The argument that some verification is performed in Olivo, referring to column 4, lines 32-36 and column 4, line 63 to column 5, line 10 (response at page 13), and thus that Olivo does not teach disabling the internal program verification operations is also not persuasive since some verification is selectively performed just as in the claimed invention (see column 2, lines 13-16 and 28-31 and claim 10, step A of Olivo and also see pages 10 and 11, lines 17-18 and claim 14 of the present application, e.g.).. Olivo teaches disabling internal (within the "memory") program testing or verification operations during a "special" test mode while permitting some verification to be selectively performed using circuits such as the just as in the claimed invention. Thus, the broad language of the claim is seen to be met.

The argument that there is no motivation to combine the teachings of the references is also not persuasive. Olivo clearly teaches that by disabling an internal program verification operation, tests can be performed in a manner fully independent of control circuitry such as the internal write state machine and various parameters may be selected at will. The ability to independently perform verification or testing operations in a flash memory fully independent of the memory control circuitry, as well as the time savings taught by the Intel Application Notes achieved by eliminating redundant verification operations, provide ample motivation and suggestion to one of ordinary skill in the art to disable internal write state machine for controlling verification operations in the flash memory system of Application Note AP-678 or Application Note AP-629, each taken separately, to arrive at a structure and method on which applicants

claims read. Thus, the invention as claimed is seen to be obvious in light of the combined teachings of the references.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187